

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.
53047/44791

In Re Application:
Indeck et al.

Serial No.
10/722,691

Filing Date
November 24, 2003

Examiner
Not Yet Assigned

Group Art Unit
2186

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Benjamin L. Volk, Jr., Reg. No. 48,017
Thompson Coburn LLP
One US Bank Plaza
St. Louis, Missouri 63101-9928
314-552-6000
314-552-7000 FAX

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TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))			Docket No. 53047/44791	
In Re Application Of: Indeck et al.				
Serial No. 10/722,691		Filing Date November 24, 2003		Examiner Not Yet Assigned
				Group Art Unit 2186
Title: Associative Database Scanning And Information Retrieval				
<p style="text-align: center;">Address to: Assistant Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450</p> <p style="text-align: center;">37 CFR 1.97(b)</p> <p>1. <input checked="" type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.</p> <p style="text-align: center;">37 CFR 1.97(c)</p> <p>2. <input type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:</p> <p style="padding-left: 40px;"><input type="checkbox"/> the statement specified in 37 CFR 1.97(e);</p> <p style="text-align: center;">OR</p> <p style="padding-left: 40px;"><input type="checkbox"/> the fee set forth in 37 CFR 1.17(p).</p>				

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	10/722,691
Filing Date	November 24, 2003
First Named Inventor	Indeck et al.
Art Unit	2186
Examiner Name	Not Yet Assigned
Attorney Docket Number	53047/44791

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	AA	WO 01/80082	10-25-2001	Indeck et al.		

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	AB	PATENT COOPERATION TREATY; International Search Report; May 6, 2004	
	AC	ARNOLD et al.; <i>The Splash 2 Processor and Applications</i> ; Proceedings 1993 IEEE International Conference on Computer Design: VLSI in Computers and Processors; October 3, 1993; pp. 482-485; Cambridge, Massachusetts	
	AD	CLOUTIER et al.; <i>VIP: An FPGA-Based Processor for Image Processing and Neural Networks</i> ; Proceedings of Fifth International Conference on Microelectronics for Neural Networks; February 12, 1996; pp. 330-336; Los Alamitos, California	
	AE	HEZEL et al.; <i>FPGA-Based Template Matching Using Distance Transforms</i> ; Proceedings of the 10 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines; April 22, 2002; pp. 89-97; USA	
	AF	MOSANYA et al.; <i>A FPGA-Based Hardware Implementation of Generalized Profile Search Using Online Arithmetic</i> ; ACM/SIGDA International Symposium on Field Programmable Gate Arrays; February 21, 1999; pp. 101-111; Monterey, California	
	AG	RATHA et al.; <i>Convolution on Splash 2</i> ; Proceedings of IEEE Symposium on FPGAs for Custom Computing Machines; April 19, 1995; pp. 204-213; Los Alamitos, California	
	AH	SHIRAZI et al.; <i>Quantitative Analysis of FPGA-Based Database Searching</i> ; Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology; May 2001; pp. 85-96; Vol. 28, No. 1/2; Dordrecht, Netherlands	
	AI	TING-PANG LIN et al.; <i>Real-Time Image Template Matching Based on Systolic Array Processor</i> ; International Journal of Electronics; December 1, 1992; pp. 1165-1176; Vol. 73, No. 6; London, Great Britain	
	AJ	VILLASENOR et al.; <i>Configurable Computing Solutions for Automatic Target Recognition</i> ; Proceedings of IEEE Symposium on FPGAs for Custom Computing Machines; April 17, 1996; pp. 70-79; Los Alamitos, California	
	AK	YAMAGUCHI et al.; <i>High Speed Homology Search with FPGAs</i> ; Proceedings Pacific Symposium on Biocomputing; January 3, 2002; pp. 271-282; Vol. 7; Lihue, Hawaii	

Examiner Signature		Date Considered	
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